IN THE SPECIFICATION

Please amend the paragraph beginning at line 7 of Pg. 9, which is corrected for consistency with the text of line 20 of Pg. 6 (i.e., no new matter has been added), as follows:

Figures 4A and 4B illustrate one embodiment of the novel printed circuit board 100 formed according to the teachings of the present invention. As can be seen in Figure 4A, which is top plan (or side cut-away) view of the circuit board 100, there is a first conductive layer 110 having an interstice 160 formed in it. The second conductive layer 120 has a second interstice 150 formed in it. The two interstices 150, 160 are engaged, or sinuously intertwined. However, between the engaged interstices 150, 160 a dielectric layer 130 is disposed. The result is that a capacitor 95 is formed in the circuit board 100 between the first and second conductive layers 110, 120 by engaging the interstices 150, 160 across the dielectric layer 130. Whereas surface mount capacitors mounted to a circuit board using prior art techniques served to take up real estate and impede board routing, the design of the board 100 allows a capacitor 95 to be formed across which circuit traces 97 may be freely routed (on other circuit layers), since the use of a surface mount capacitor and through-hole vias are now obviated due to the capacitance thereby provided.

IN THE DRAWINGS

Proposed corrected drawings, as requested in the Office Action, are supplied herewith. All figures have been corrected with red ink to show that only twelve pages of drawings are presented for examination, rather than thirteen pages. Originally-presented page 9 of 13 (a duplicate of the current page 8 of 12) has been deleted.

In addition, Figures 2-4A, and 5-17 have been corrected with red ink to remove unecessary cross-hatching in the interest of clarity. However, it should be noted that in several of the figures (e.g., Figures 4A, 5-11, 13, and 16-17), the illustration may be of both a top, plan view and a side, cut-away view (in which case additional cross-hatching could be properly shown for several elements of the various embodiments).

Finally, please note the red ink changes to Figures 14 and 15. The interstices 150 and 160 have been clearly marked, to correspond with the side, cut-away views of Figures 13 and 16. The broken lines indicate the presence of the interstices 150, 160 beneath the surface of the conductive layer 120 and/or the dielectric layer 130.